

JUN 04 2004
OFFICIAL

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: DEBASHIS BHATTACHARYA
Serial No.: 09/898,071
Filed: JUNE 29, 2001
For: PROCESS FOR AUTOMATED GENERATION OF DESIGN-
SPECIFIC COMPLEX FUNCTIONAL BLOCKS TO IMPROVE
QUALITY OF SYNTHESIZED DIGITAL INTEGRATED
CIRCUITS IN CMOS
Art Unit: 2825
Examiner: DO, THUAN V.
Confirmation No.: 9529
Customer No.: 27623
Attorney Docket: 162.7106USU

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR RECONSIDERATION

Sir:

In reply to the Office Action dated March 4, 2004, please enter and
consider the following remarks in the above-identified patent application:

Remarks begin on page 2 of this paper.